Product Functional Specification
(RoHS-Compliant)

15 inch XGA Color TFT LCD Module
Model Name : B150XG01 V.8

( ) Preliminary Specification
(◆) Final Specification

Note: This Specification is subject to change without notice.

I. Contents

II Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1. 2005/3/3	All	First release	All	
0.2. 2005/4/7	1		RoHS-Compliant	
0.2. 2005/4/7	17		Update Power on/off sequence	
0.3. 2005/6/1	20		Add EDID	
0.4. 2005/6/23	5	317.3 x 242.0 x 6.0 (max.)	317.3 (typ.) x 242.0 (typ.) x 6.0 (max.)	Final spec

1.0 Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2.0 General Description

This specification applies to the 15.0 inch Color TFT/LCD Module B150XG01.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

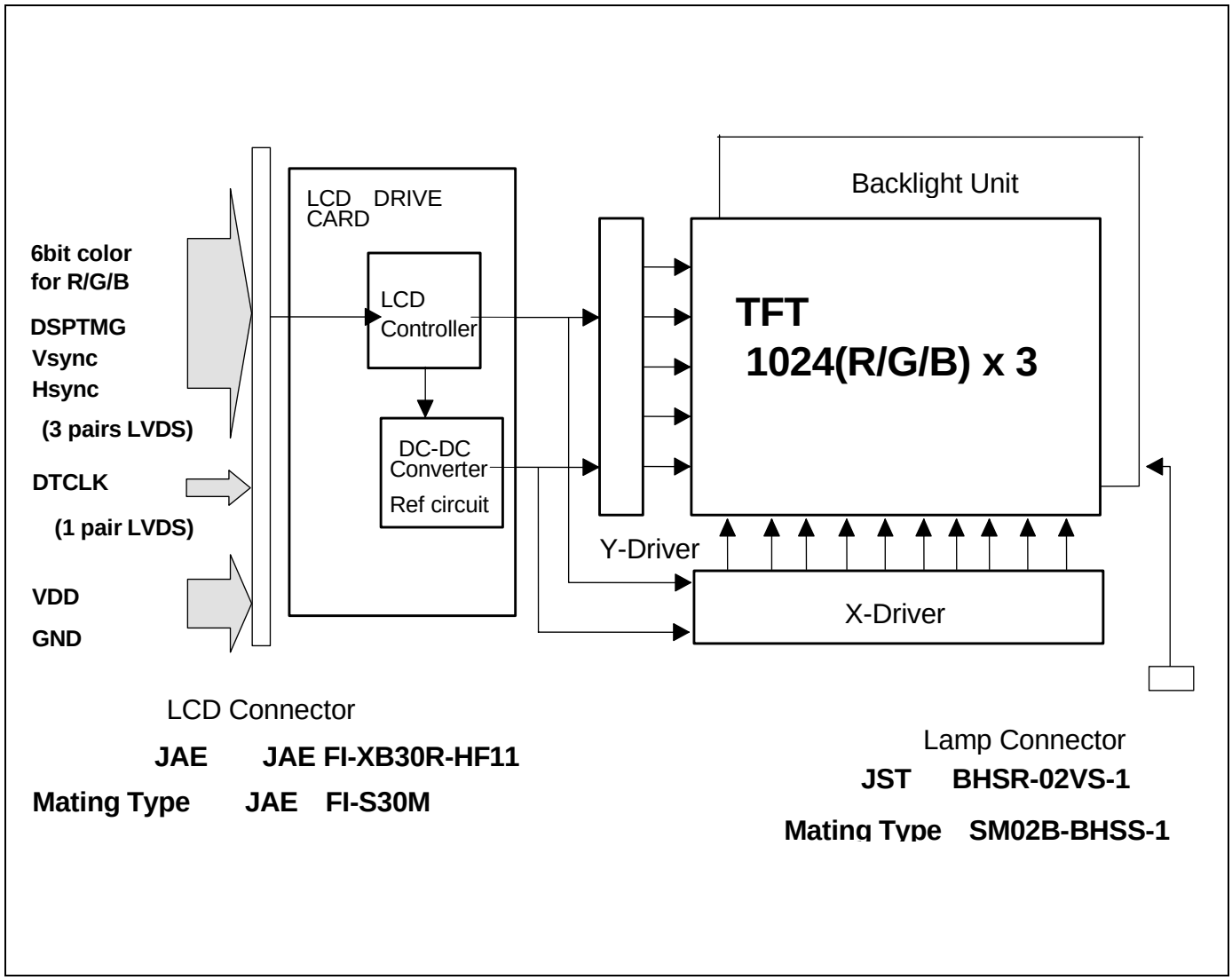
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	381
Active Area	[mm]	304.1 X 228.1
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.297X0.297
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	150 (5 point minimum) 180 (5 point average)
Luminance Uniformity		1.25 max. (5 pts) 1.65 max. (13pts)
Contrast Ratio		300
Optical Rise Time/Fall Time	[msec]	24/11
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.6W
Weight	[Grams]	550g typ.
Physical Size	[mm]	317.3 (typ.) x 242.0 (typ.) x 6.0 (max.)
Electrical Interface		1 channel LVDS
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60
Surface Treatment		3H (Glare)

2.2 Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1150	Vrms	
Operating Temperature	TOP	0	+50	[^{o}C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[^{o}C]	Note 1
Storage Humidity	HST	5	95	[%RH]	Note 1
Vibration			1.5 10-500 (random)	G Hz	2hr/axis, X,Y,Z
Shock			220 , 2	G ms	Half sine wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item		Conditions	Typ.	Note
Viewing Angle K: Contrast Ratio	[degree] [degree] [degree] [degree]	Horizontal (Right) K = 10 (Left) Vertical (Upper) K = 10 (Lower)	40 40 10 30	—-— — —
Contrast ratio			300	—
Luminance Uniformity			1.25 max. (5 pts) 1.65 max. (13pts)	
Response Time (Room Temp.)	[msec] [msec]	Rising Falling	24 11	15(Max.) 30(Max.)
Color Chromaticity Coordinates (CIE)		Red x Red y Green x Green y Blue x Blue y White x White y	0.576+-0.03 0.326+-0.03 0.315+-0.03 0.542+-0.03 0.149+-0.03 0.135+-0.03 0.313+-0.03 0.329+-0.03	
White Luminance (CCFL 6.0 mA)	[cd/m^2]		150 (5-point minimum) 180 (5 points average)	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SR-HF11 or compatible
Mating Housing/Part Number	FI-X30M, FI-X30C or FI-X30H
Mating Contact/Part Number	FI-C3-A1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VEDID
5	NC	6	CLKEDID
7	DATAEDID	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20	GND
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC

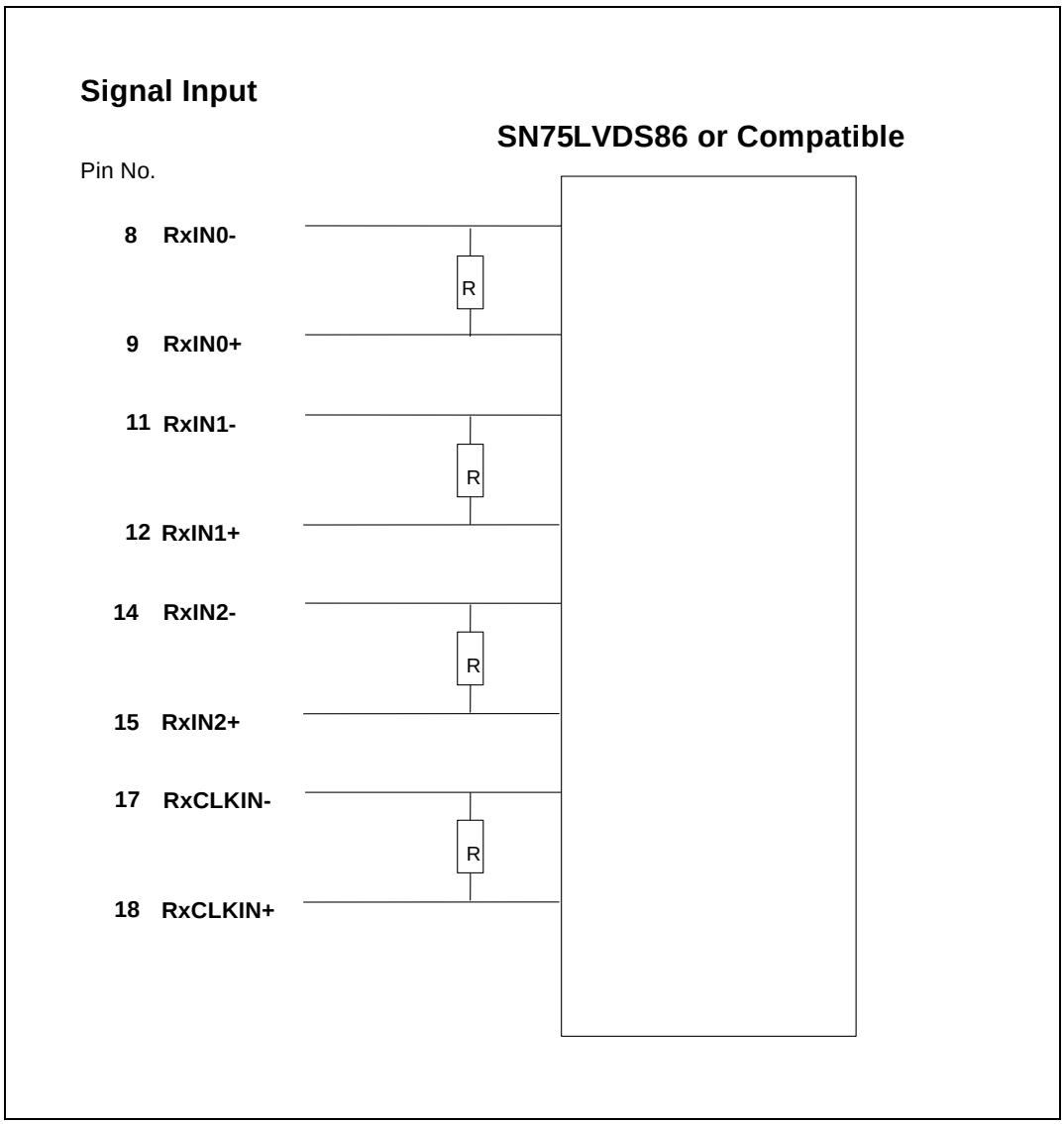
5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.

GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 54.0 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

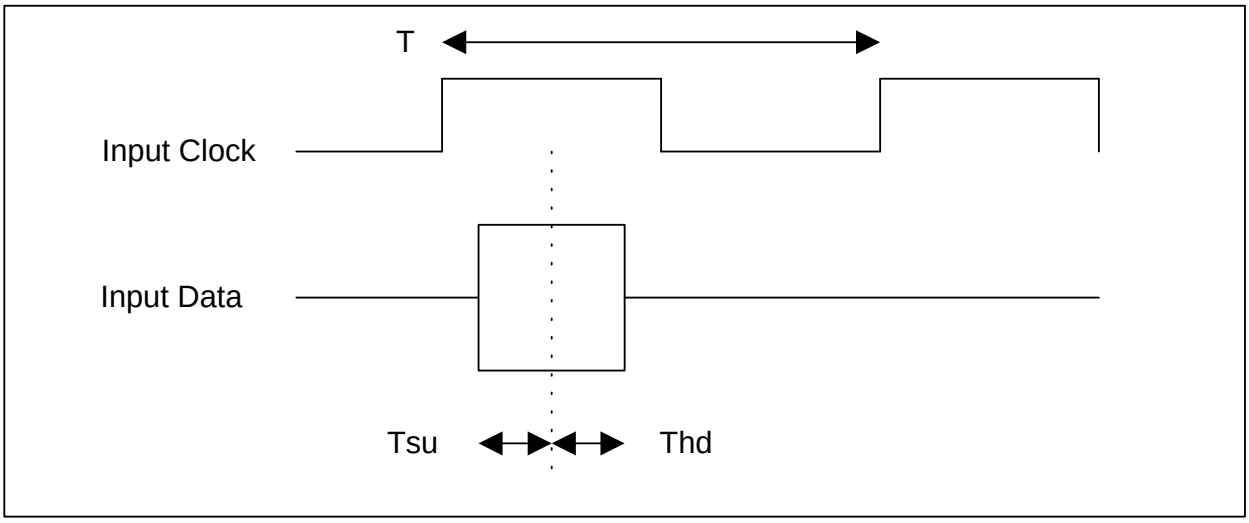
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	50MHZ	68MHZ
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	

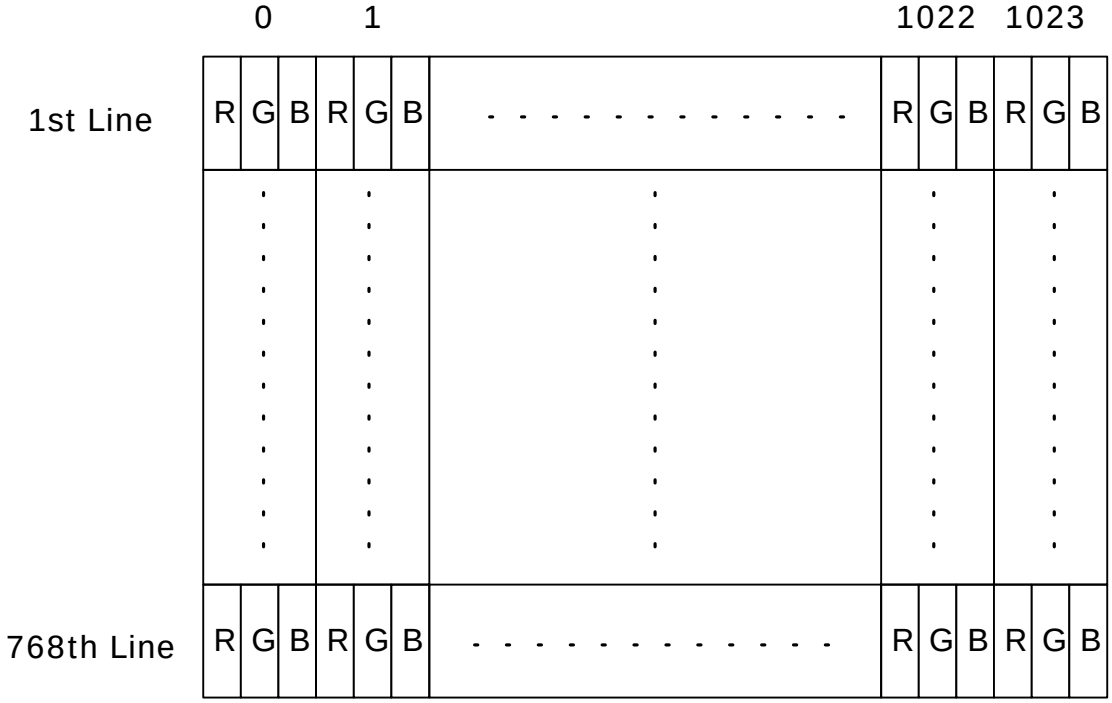


5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CFL Inverter

Parameter	Min-	DP-1	Max-	Units	Condition
White Luminance 5 points average	-	180	—	[cd/m^2]	(Ta=25°C)
CCFL current(ICFL)	3.0-	6.0	7.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(FCFL)	40	50	60	[KHz]	(Ta=25°C) Note 3
CCFL Ignition Voltage(Vs)		—	1,150	[Volt] rms	(Ta= 0°C) Note 4
CCFL Voltage (Reference) (VCFL)	—	700	—	[Volt] rms	(Ta=25°C) Note 5
CCFL Power consumption (PCFL)	—	4.2	—	[Watt]	(Ta=25°C) Note 5

Note 1: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be emplyed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.
Note 3: CFL discharge frequency should
be carefully determined to avoid interference between inverter and TFT LCD.
Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.
Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

8.0 Interface Timings

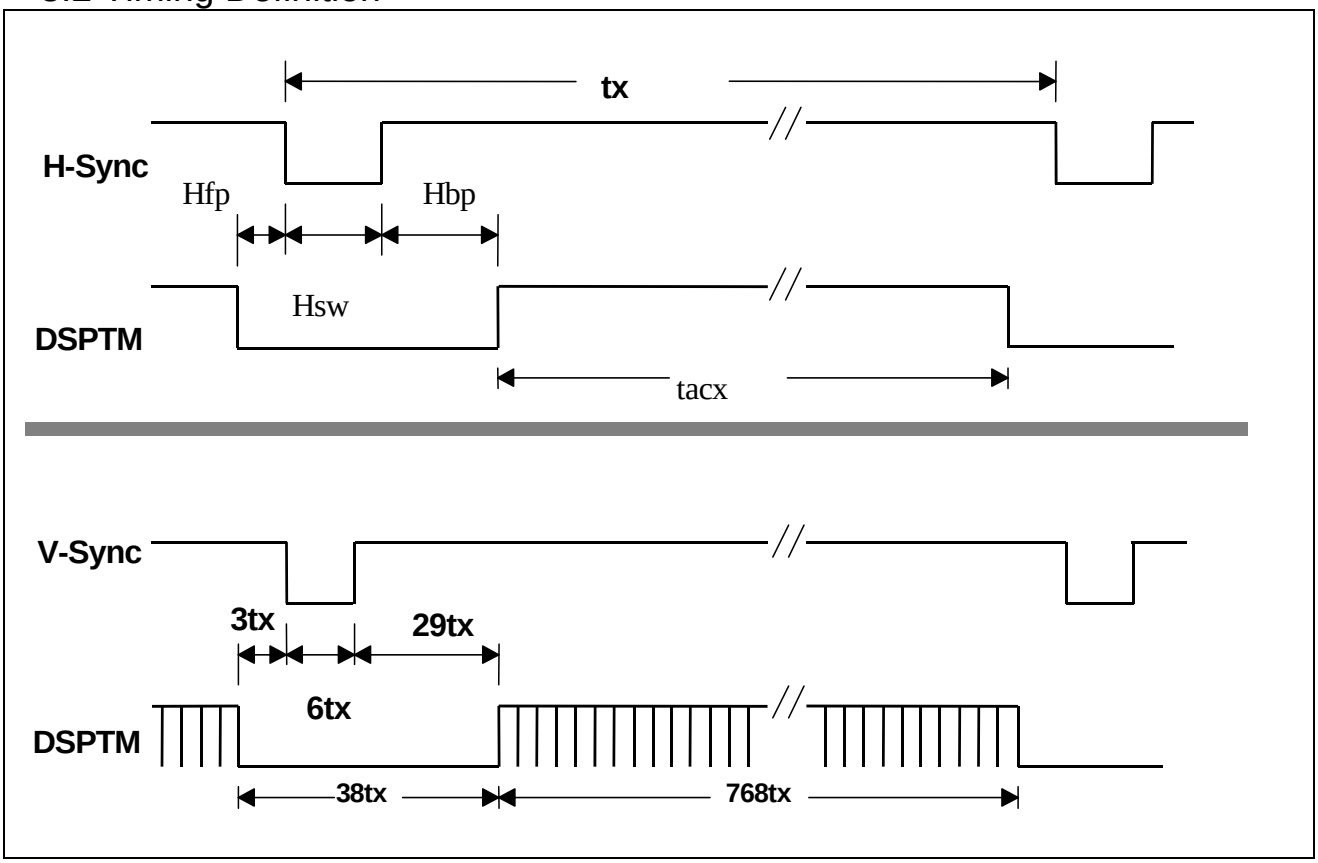
Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency	**50**	65.00	**68**	[MHz]
tck	DTCLK cycle time		15.38		[nsec]
tx	X total time	1206	1344	1648	[tck]
tacx	X active time		1024		[tck]
tbkx	X blank time	90	320		[tck]
Hsync	H frequency		48.363		[KHz]
Hsw	H-Sync width	2	136		[tck]
Hbp	H back porch	4	160		[tck]
Hfp	H front porch	8	24		[tck]
ty	Y total time	771	806	895	[tx]
tacy	Y active time		768		[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	2	6		[tx]
Vfp	V-sync front porch	1	3		[tx]
Vbp	V-sync back porch	7	29	63	[tx]

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition



9.0 Power Consumption

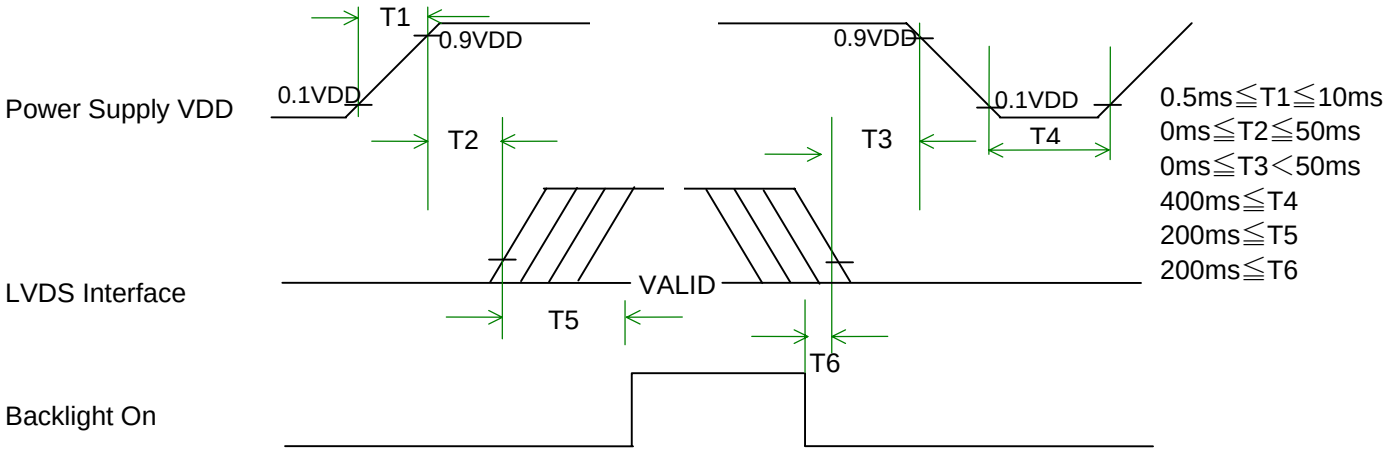
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.26		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.91	[Watt]	Max Pattern Note
IDD	IDD Current		380		mA	All Black Pattern
IDD Max	IDD Current max			580	mA	Max Pattern Note
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

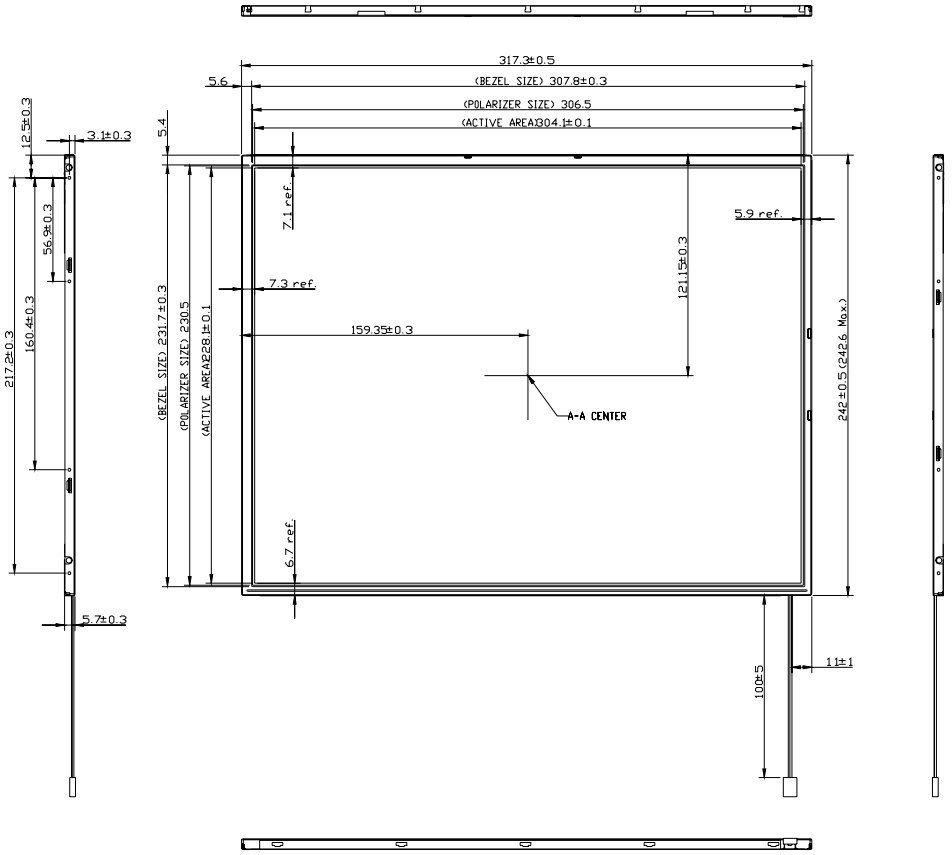
Note : VDD=3.3V

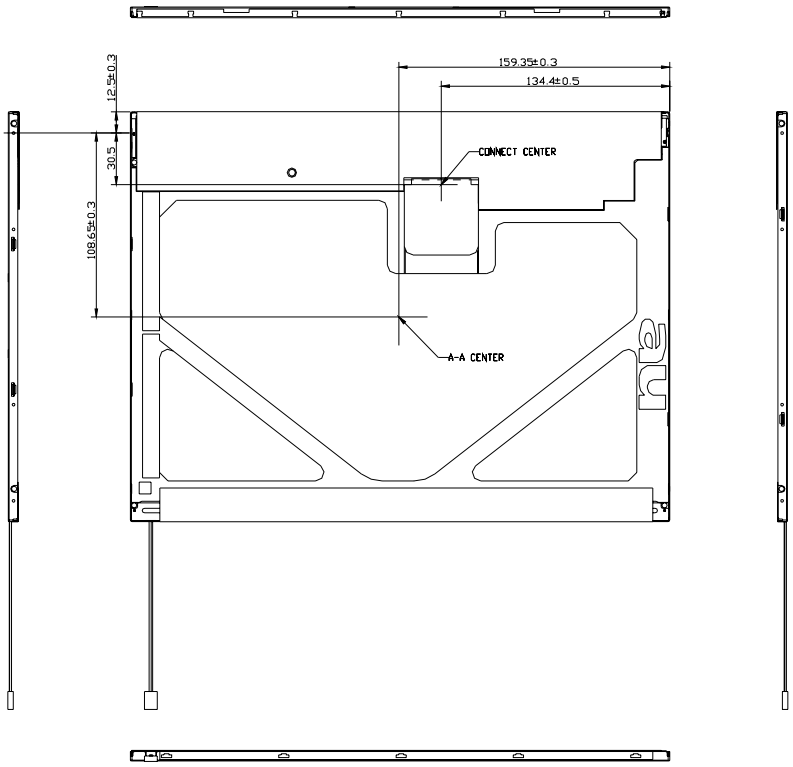
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





12.0 EDID table

B150XG01 V8 EDID Table

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC	Notes
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	51	01010001	81	Panel size and resolutiion
0B	hex, LSB first	18	00011000	24	Model and version number
0C	32-bit ser #	00	00000000	0	Fix number
0D		00	00000000	0	Fix number
0E		00	00000000	0	Fix number
0F		00	00000000	0	Fix number
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	0E	00001110	14	Value = Year -1990
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	02	00000010	2	
14	Video input definition	80	10000000	128	Digital signal level
15	Max H image size	1E	00011110	30	30cm
16	Max V image size	17	00010111	23	23 cm
17	Display Gamma	78	01111000	120	Gamma 2.2
18	Feature support	0A	00001010	10	NO DPMS,Active off,RGB,timing BLK 1,NO GTF
19	Red/green low bits	12	00010010	18	
1A	Blue/white low bits	E5	11100101	229	
1B	Red x/ high bits	91	10010001	145	Rx=0.566
1C	Red y	52	01010010	82	Ry=0.321
1D	Green x	52	01010010	82	Gx=0.320
1E	Green y	89	10001001	137	Gy=0.537
1F	Blue x	27	00100111	39	Bx=0.155

20	Blue y	24	00100100	36	By=0.143
21	White x	50	01010000	80	Wx=0.313
22	White y	54	01010100	84	Wy=0.329
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Detailed timing/monitor	64	01100100	100	65Mhz
37	descriptor #1	19	00011001	25	1024x768 @60Hz
38		00	00000000	0	Hor active=1024 pixels
39		40	01000000	64	Hor blanking=320pixels
3A		41	01000001	65	
3B		00	00000000	0	Vertcal active=768 lines
3C		26	00100110	38	Vertical blanking=38lines
3D		30	00110000	48	
3E		18	00011000	24	Hor sync. Offset=24 pixels
3F		88	10001000	136	H sync. Width=136 pixels
40		36	00110110	54	V sync. Offset=3 lines
41		00	00000000	0	V sync. Width=6 lines
42		30	00110000	48	H image size= 304.1 mm
43		E4	11100100	228	V image size = 228.1 mm
44		10	00010000	16	
45		00	00000000	0	Horizontal Border = 0 pixels
46		00	00000000	0	Vertical Border = 0 lines
47		18	00011000	24	

48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		06	00000110	6	HSPW min=12
4E		77	01110111	119	HSPW max=238
4F		08	00001000	8	Thbp min=16
50		FF	11111111	255	Thbp max=620
51		01	00000001	1	VSPW min=2
52		0F	00001111	15	VSPW max=30
53		05	00000101	5	Tvbp min=9
54		2E	00101110	46	Tvbp max=93
55		2D	00101101	45	Thp min=1114
56		FF	11111111	255	Thp max=1648
57		05	00000101	5	Tvp min=778
58		3F	00111111	63	Tvp max=895
59		01	00000001	1	Module revision
5A	Detailed timing/monitor	00	00000000	0	Ascii Data String: AUO
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F		41	01000001	65	A
60		55	01010101	85	U
61		4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	Monitor Name: B150XG01V8
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	

70		00	00000000	0	
71		42	01000010	66	B
72		31	00110001	49	1
73		35	00110101	53	5
74		30	00110000	48	0
75		58	01011000	88	X
76		47	01000111	71	G
77		30	00110000	48	0
78		31	00110001	49	1
79		56	01010110	86	V
7A		38	00111000	56	8
7B		0A	00001010	10	
7C		20	00100000	32	
7D		20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	83	10000011	131	